System-on-a-Chip Design of Self-Powered Wireless Sensor Nodes for Hostile Environments

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Abstract—A new dimension of wireless sensor network architecture design is emerging where hundreds to thousands of ultra-light (<10 g) low-cost sensor nodes are required to collectively perform a spectrum of distributed remote sensing missions in hostile conditions, predominantly those encountered in space. Environmental extremes, such as mechanical, thermal, atmospheric, energetic, and dynamic must be considered. Research is underway to investigate the feasibility of fabricating survivable self-powered wireless sensor nodes monolithically with commercially available complementary metal-on-silicon technology. An example "SpaceChip" scenario is presented, where the conceptual design of a satellite-on-a-chip is explored. [1, 2]

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1. INTRODUCTION

A new dimension of wireless sensor network architecture design is emerging where hundreds to thousands of ultra-light (<10 g) low-cost sensor nodes are required to collectively perform a spectrum of distributed remote sensing missions in hostile environments, predominantly those encountered in space. This paper presents a novel approach to meet these stringent requirements.

The satellite-on-a-chip idea has sparked a lot of interest in the space community, since the first known mention of the concept in 1994 [1]. We recently completed a satellite-on-a-chip feasibility study, based on a monolithic system-on-a-chip (SoC) design, but the lack of viable applications discouraged further development initially [2]. In response, the future need for low-cost mass-producible very small satellites for distributed space missions was examined [3].

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The smallest silicon-based mass-producible technique for satellite fabrication was proposed by Janson and Helvajian from the Aerospace Corporation in 1999 [4]. Well beyond the scope of SoC, the vision was to build satellites out of stacks of silicon wafers processed by complementary metal-on-silicon (CMOS), microelectromechanical system (MEMS), and photovoltaic foundries. Their team has since pioneered a range of small satellite manufacturing technologies [5]. The high cost of commercializing these processes has prevented widespread implementation.

The Surrey Space Centre set a long-term goal in 1999 of developing and flying the world's first satellite-on-a-chip, based on a true stand-alone SoC approach. Since that time, they have facilitated numerous research efforts towards that goal. The monolithic SoC approach has been challenged by various packaging alternatives, including traditional printed circuit board (PCB), multichip module (MCM), system-in-package (SiP), and now system-on-package (SOP); however, SoC's attraction is its low cost and mass-producibility [6].

Related prototyping design activities have been undertaken, targeting a system mass less than one kilogram, leading to a 70 g satellite-on-a-PCB prototype. This very small satellite design, named PCBSat, has given insight into various aspects of satellite system development on a very small scale. Although developed as a prototype, it gives rise to a promising cost-effective mass-producible solution for certain large-scale distributed space missions [7].

Satellite-on-a-chip has gained new appeal in the context of space sensor networks [3]. Nearly all wireless sensor network applications to date have been for relatively benign terrestrial environments, with a few exceptions where thermal extremes are concerned [8].

The paper is structured as follows. The next section expands the wireless sensor network discussion by giving a more in-depth background of the topic and associated sensor node technology development. Section 3 presents a generalized set of design requirements and proposes solutions based on contemporary ideas in the literature. Section 4 applies these potential solutions by presenting a satellite-on-a-chip application example. The paper concludes with a roadmap of future research required to realize a true stand-alone SoC wireless sensor node for hostile environments.

2. SENSOR NODE BACKGROUND

The wireless sensor network concept emerged in the early 1990's, with academic roots that can be traced through an original group of researchers at the University of California, Los Angeles [9]. Various terms have been used to describe this concept over the past decade, but "wireless sensor networks" has endured. In addition to developing the theory and supporting software, three hardware solutions for sensor nodes, sometimes called motes, were initially pursued: Smart Dust, commercial off-the-shelf (COTS) Dust, and Wireless Integrated Sensor Networks (WINS).

Although the actual idea of Smart Dust was born at a 1992 U.S. military workshop, Pister [10] is credited with coining the phrase and the first major development, shortly after leaving UCLA for Berkeley. The first Smart Dust implementation was a battery-powered MCM featuring a MEMS corner cube reflector for optical communications [11]. Pister's team went on to demonstrate a solar-powered variant soon after, as shown in Figure 1 [12].

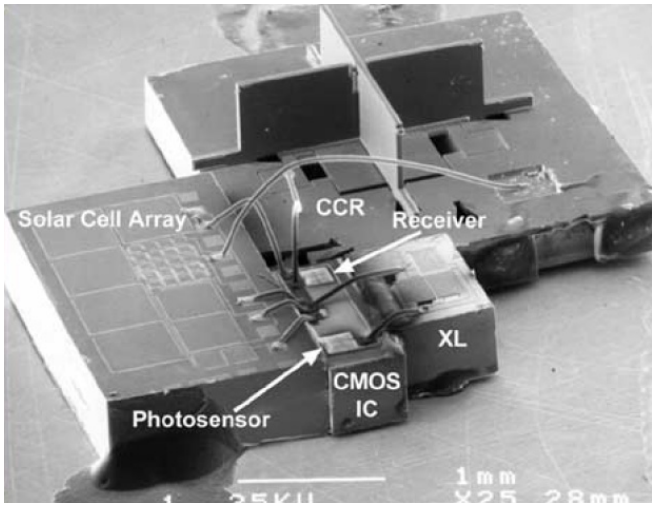

Figure 1. Smart Dust

The new Berkeley team developed COTS Dust in parallel to Smart Dust. As shown in Figure 2, this concept was based on a PCB substrate, with three versions utilizing radio frequency (RF) communications while one used optical [13]. Spin-off companies emerged, such as Crossbow, which now sell the popular MICA family of motes. To simplify their implementation, the TinyOS operating system is now widely used in most motes.

While Smart Dust was in development, four of the original UCLA academics, led by Kaiser [14], pursued an RF-based SoC called WINS. Upon closer inspection, their approach was actually based on MCM integration of a sensor, microprocessor, and transceiver; which is similar to optical Smart Dust, but uses an RF link. Kaiser went on to lead further integrated RF work in CMOS; however, no recent work on WINS has been published in the literature.

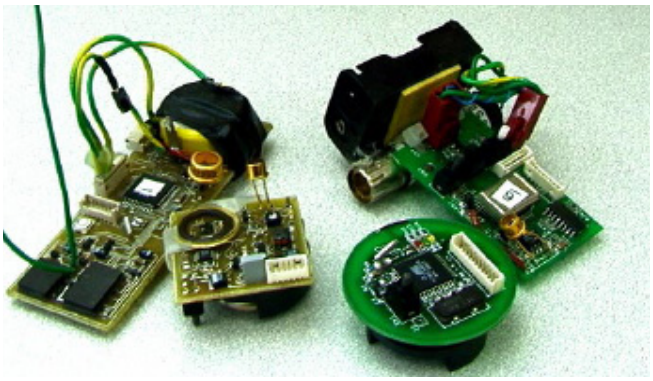

Figure 2. COTS Dust

One of the most promising SoC projects is WiseNET, which has successfully integrated a radio, microprocessor, data storage, power control, and analog interface, as shown in Figure 3 [15]. Although closer to a true SoC solution, the WiseNET sensor node still requires numerous external components, including a power source, passive devices, an antenna, and sensor.

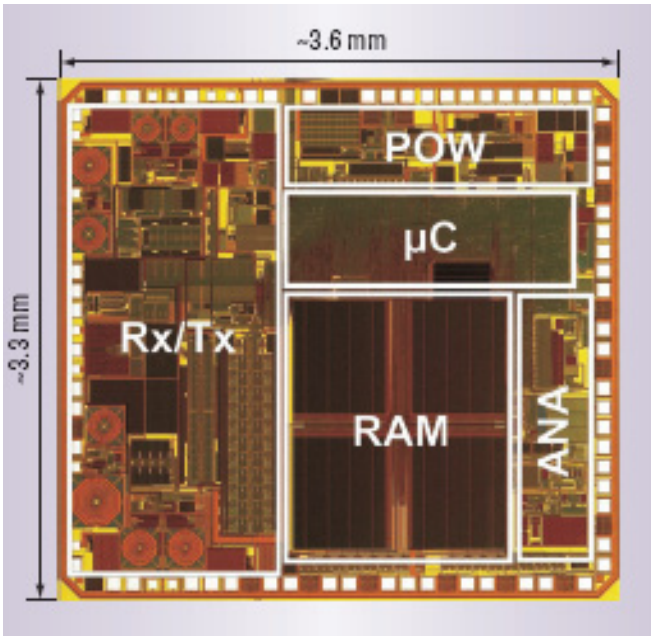

Figure 3. WiseNET SoC Sensor Node

In response to WiseNET, The Smart Dust team recently published a comprehensive investigation of an RF-based SoC approach [16]. It includes a discussion on the remaining work to realize a complete stand-alone SoC implementation. They concluded that although recent SoC solutions have demonstrated increased monolithic integration, many large off-chip components are still required, such as a sensor, battery, passives, crystal clock source, and RF antenna. Completed during the same period, our satellite-on-a-chip feasibility assessment, with similar objectives, arrived at the same conclusions [3].

3. SURVIVABLE SOC NODE REQUIREMENTS

In this section, we discuss functional requirements for a self-powered SoC sensor node design aimed at hostile environments. A range of potential solutions for a generalized set of functional requirements is presented, focusing on the following aspects:

- Missions and sensors
- System configuration
- Power generation, storage, distribution, and control
- Data handling, processing, and storage
- Wireless communications with other nodes
- Environmental operability and survivability

Missions and Sensors

A range of potential missions has been previously explored for hostile environments, focusing on space, such as real-time upper atmospheric monitoring [3]. Depending on the selected mission, appropriate sensors must be chosen. In pursuit of the most complete SoC solution, one must consider all currently available on-chip technologies.

Visible imagers are the most common sensor integrated on CMOS [17], but for most space applications, they are the least useful at this scale. They also require a lens. Other monolithic CMOS sensor technologies were investigated, such as simple infrared, magnetic, and pressure sensors [18].

Recently, a wide range of sensors has emerged, based on "CMOS-MEMS" technology. However, CMOS-MEMS requires custom pre-, front-end, and/or back-end processing. Of these three methods, back-end bulk micromachining of CMOS has been the most successful. Numerous sensors have been demonstrated, such as pressure, chemical, thermal, tactile, proximity, flow, force, neural, vacuum, acceleration, gyroscopic, sound, and infrared [19]. Due to its growing popularity, a few commercial foundries now offer limited CMOS-MEMS processing, such as X-FAB.

System Configuration

Compared to PCB, MCM, SiP, or SOP approaches, a strict monolithic SoC pursuit imposes some formidable limitations. Most notably, the design cannot exceed the reticle, which is an area limit dictated by the photolithography process used in the particular process line. This limits the maximum circuit area to approximately 360 mm^2 for modern processes, which grows in time as the technology matures. Assuming a silicon density of 2330 kg/m^3 and wafer thickness of 0.75 mm, the die mass would be approximately one gram. In addition, process incompatibilities determine the degree of monolithic integration. Although SoC architectures are rather inflexible, the potential for low cost and mass producibility often makes it the most attractive. Full-reticle prototypes can cost up to $10,000 each, but a commercial production run could drive the unit cost well below $500.

Power Generation, Storage, Distribution, and Control

Power distribution, regulation, and control aspects of an on-chip power system can be met with basic wiring, switching, and regulation circuitry in CMOS [20]. The challenge lies in monolithic power generation and storage via solar, chemical, nuclear, mechanical, or electromagnetic sources. Recent "micro power" research has presented several new integrated options for SoC applications.

Solar cells are typically fabricated with dedicated silicon or gallium arsenide processes, incompatible with commercial CMOS. MCM integration is a typical solution used for miniature systems. Pister [21], confronting this limitation, successfully pursued monolithic integration of solar cells, CMOS, and MEMS using custom silicon-on-insulator (SOI) processing. However, SOI is not yet widely available. Monolithic CMOS solar cell integration has only recently been demonstrated with marginal results. Three such examples are a microprocessor, reporting an efficiency of 1% (far below 15% for typical silicon cells) [22], artificial vision implants [23], and basic research [24]. There are no known solar-thermal conversion techniques for SoC.

A monolithically integrated chemical fuel cell has been demonstrated with an operating time of 170 hours and mean open-circuit voltage of 0.533V [25]. Unfortunately, it relies on an oxygen-rich atmosphere, which is not suitable for space, but will work terrestrially. Other micro chemical power supplies, such as thin-film batteries, nuclear batteries, and microturbines have been investigated, but none can be monolithically integrated.

Mechanical energy is typically converted by electromechanical generators, but piezoelectric power generation is also possible. Work is underway in piezoelectric micro power sources, but not yet for SoC [26]. Another promising source of integrated electrical power is through inductive energy transfer. This has been shown in a monolithic SoC for medical implants [27].

Data Handling, Processing, and Storage

The heart of a wireless sensor node is typically a COTS microcontroller with a small amount of volatile memory and an analog-to-digital converter (ADC). The ADC usually serves as the sensor interface. Most COTS-based nodes use the TinyOS operating system. To save power, the microcontroller is clocked at a slow rate with an external oscillator and sleep modes are used when possible.

Asynchronous SoC architecture, which offers numerous advantages, has not yet been considered by this niche community. Typically, asynchronous implementations only require 25-30% of the power of their clocked counterparts, produce very little electromagnetic interference (EMI), and

do not require an external oscillator. Asynchronous designs are event triggered, processing new data using the minimum number of gate transitions possible. Asynchronous SoC design also promises to solve the global clock delay problem, which increases as the size of SoCs grow with increased functionality and performance [28].

Wireless Communications with Other Nodes

The original Smart Dust design presented in [10] used optical communications to take advantage of its power efficiency. Optical links are also free of regulatory issues and can use simple on/off keying (OOK) modulation schemes. This approach is only effective in line-of-sight situations where the alignment is controlled. For sensor networks within a larger spacecraft, line of sight would be difficult. For free-flying nodes, the alignment problem becomes the predominant issue.

Low-power on-chip transceivers have become the preferred choice for sensor nodes. SoC transceivers, which were a novelty only a few years ago [29] are now commercially available, some even with an integrated microcontroller. The commercial availability of RF CMOS and SiGe BiCMOS processes has offered increased capabilities, including a wider selection of operating frequencies [30]. SoC transceivers still require external passive elements, crystal oscillators, and an antenna.

In an effort to eliminate external antennas, on-chip antennas have been investigated. The maximum range achieved is approximately five meters, as demonstrated by Lin [31] and O [32]. Their experiments used frequencies greater than 10 GHz to ensure that a quarter-wavelength antenna would fit on a chip. On-chip antennas for the 900 MHz and 2.4 GHz Instrumentation, Scientific, and Medical (ISM) bands would be cost prohibitive, requiring the full reticle for any design.

Environmental Operability and Survivability

Wireless sensor node solutions have not yet been considered for hostile conditions, specifically for those encountered in space and terrestrial industrial settings. The following five environmental hazard categories are introduced and discussed further.

(1) Mechanical (shock, vibration, acceleration)

(2) Atmospheric (corrosion, debris, vacuum)

(3) Thermal (extremes, limited heat transfer)

(4) Energetic (radiation, including charged particles)

(5) Dynamic (free-fall orbit, high velocity mobility, attitude disturbance torques)

Mechanical (shock, vibration, acceleration)—Fragile MEMS structures are not suitable for applications where excessive shock, vibration, and/or acceleration may exist. These hazards are seen in the space launch segment and industrial process plants. The mechanical rigidity of a monolithic SoC is far superior in this case.

Atmospheric (corrosion, debris, vacuum)—Corrosion is an issue for low-Earth orbit (LEO), industrial/chemical, and biomedical applications. Any exposed aluminum on a SoC must be covered, either by gold plating or by passivation [33]. Space debris is normally considered a hazard for satellites, but for a mission where thousands of objects are put in space, they become a big concern to other systems. The only realistic way to solve this problem is to confine these missions to LEO, where the orbital lifetime is very short, essentially making these missions disposable. Finally, the vacuum of space introduces several issues, such as cold welding and outgassing, but for SoC, the only concern is limited heat transfer.

Thermal (extremes, limited heat transfer)—Thermal extremes and cycling are exacerbated in a vacuum, as thermal radiation is the only method available for heat transfer. Silicon wafer thermal properties are well understood and certain packaging materials can be used to manage the temperature extremes for a SoC [34]. For example, space-qualified paraffin can be used to absorb heat during the sunlit portion of an orbit, and then keep the system warm during eclipse, effectively narrowing the temperature range the SoC will experience.

Energetic (radiation, including charged particles)—Extreme radiation conditions are usually experienced in nuclear power plants, certain industrial process plants, and in space. However, during the early days of integrated circuit development, high-energy alpha particles from impurities in plastic packaging turned out to be the cause of mysterious single-event upsets (SEUs) in terrestrial systems. More recently, neutrons have caused SEUs in airplane avionics systems flying at normal cruising altitudes. Simple material changes and shielding are applied in these relatively benign situations [35].

Space and nuclear reactor environments are more challenging, where ionizing radiation causes gradual system degradation as the dose accumulates. In addition, high-energy particles, such as electrons, protons, and heavy ions, can cause single event phenomena, including SEUs [35].

The problem can be solved for SoC applications at the integrated circuit level using a CMOS device layout technique called “design hardening.” This mitigates both total ionizing dose and single event phenomena as illustrated in Figure 4 [36]. Design hardening is not without fault, as there are power and area penalties. By laying out the n-type transistors in an annular shape, the mechanisms that cause transistor leakage from ionizing radiation are nearly eliminated. Increasing the drive strength (width) of the transistors increases the SEU threshold to high-energy particle strikes. Finally, adding p+ and n+ highly doped

guard rings around the transistor areas prevent single event latchup (SEL).

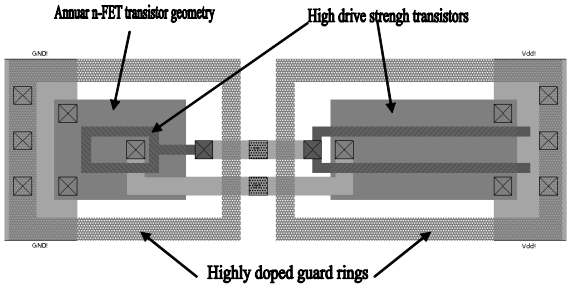

Figure 4. Layout-Based Design Hardening

Dynamic (free-fall orbit, high velocity mobility, attitude disturbance torques)—Terrestrial sensor networks are composed of relatively fixed nodes. In contrast, orbital velocity in LEO is approximately 7.5 km/s. Natural, but undesirable perturbations change the orbit over time, altering the arrangement of nodes, which is called a constellation. This factor must be fully understood, so key parameters like communication range can be selected properly. The freefall environment also presents unique challenges. The dominant effect is that objects in orbit "float" and change their orientation or "attitude" based on perturbations from solar pressure, gravity gradients, magnetic fields, and aerodynamic drag. This may not be an issue if the sensor technology does not have pointing requirements. However, if attitude control is required, SoC solutions are very challenging at this scale.

4. APPLICATION EXAMPLE: SPACECHIP

SpaceChip is the name of the first monolithic satellite-on-a-chip endeavor, investigated as a solution for distributed missions requiring large numbers of satellite nodes [3]. The core of the analysis is based on Space Mission Analysis and Design (SMAD) principles [37]. Furthermore, solutions for hostile environments are discussed.

SpaceChip Mission and Sensors

SpaceChip is a technology demonstration mission. A CMOS imager was selected to show proof-of-concept of an integrated sensor. Integrated microlenses are being considered in lieu of an off-chip lens [38].

The initial operations concept is to deploy a number of SpaceChips from a host small satellite in LEO. The mission will be performed within a very short period after separation, due to the effects of differential drag on the host satellite and the fleet of SpaceChips. The host satellite will relay the space network data to the ground. Alternatively, SpaceChip could be used in a "stick-on" fashion to deploy a wireless sensor network within a satellite, or could be used for planetary surface exploration.

SpaceChip System Configuration

A satellite is composed of a payload and a set of supporting subsystems, including: structural, electrical power (EPS), data handling (DH), communications (Comm), attitude/orbit control (AOCS), and thermal control (TCS), depending on mission requirements. A notional SpaceChip system configuration is shown in Figure 5.

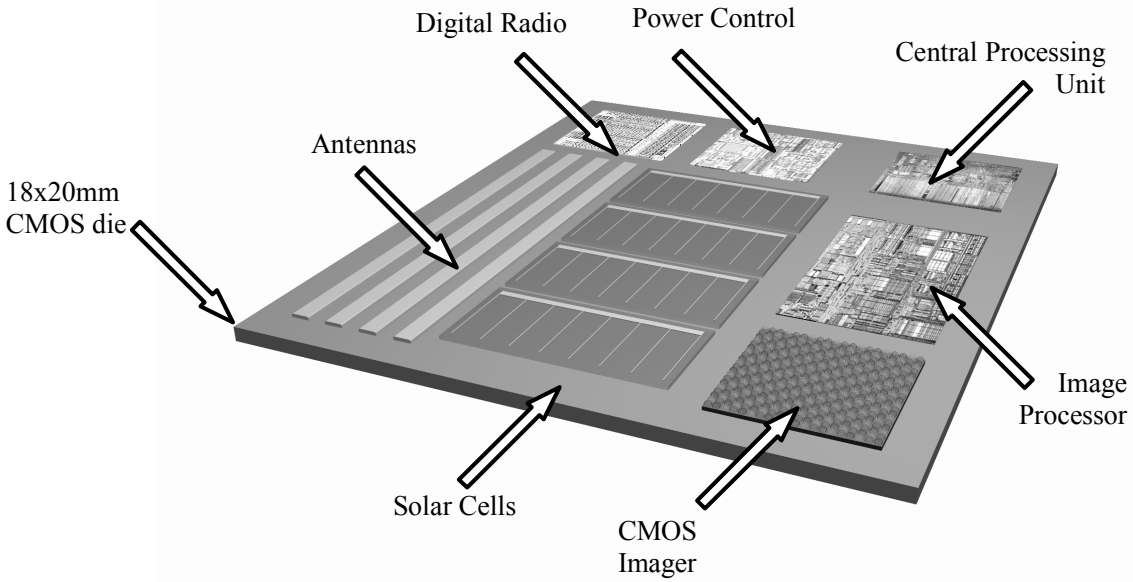

Figure 5. Notional SpaceChip System Configuration

Since the beginning of SpaceChip's development, the focus has been on a monolithic SoC architecture, with the least amount of external components possible. This limits the maximum circuit area to approximately 360 mm^2 for modern CMOS processes and a mass of one gram. As the design developed, complications dictated minimal packaging and one external component. The maximum total mass of SpaceChip is estimated to be less than 10 g.

SpaceChip Electrical Power Subsystem

Using a baseline value of 80 µW for the payload [17], Table 1 presents the power budget, which totals 1.13 mW, dominated by the communication subsystem. All other subsystem power requirements are based on the typical values for small satellites [37]. With this initial power budget, the SMAD sizing process of the EPS was accomplished with results shown in Table 2.

Table 1. SpaceChip Power Budget

System	Typical	Design	Units
Payload	40%	80	µW
EPS	15%	30	µW
DH	10%	10	µW
Comm	30%	1	mW
ADCS	5%	10	µW
Propulsion	0%	0	
Thermal	0%	0	
Structure	0%	0	
Total	**100%**	**1.13**	**mW**

Beginning with basic orbital parameters, the period, time in eclipse, and sunlit times are computed in Eq. 1–3. Required on-chip energy storage was computed in Eq. 4 and the required solar array area was computed in Eq. 5–6.

$$P = 2\pi\sqrt{\frac{a^3}{\mu_\oplus}} \tag{1}$$

$$\rho = \sin^{-1}\left(\frac{R_\oplus}{R_\oplus + h}\right) \tag{2}$$

$$T_e = \frac{2\rho}{360^\circ}P \tag{3}$$

$$w = \frac{1}{2}Cv^2 \tag{4}$$

$$P_{sa} = \left(\frac{P_d T_d}{X_d} + \frac{P_e T_e}{X_e}\right)/T_d \tag{5}$$

$$P_{BOL} = G_s \eta I_d \cos\theta \tag{6}$$

Two key findings emerged: the solar array required for this scenario is 12x12 mm, but power storage in a monolithic capacitor will not be possible. The area required for such a device, assuming a CMOS process capacitance of 4.8 $fF/\mu m^2$, is 40,000 times the maximum die area. The solar cell area requirement would consume about 40% of a full reticle die, leaving ample room for other components.

Table 2. SpaceChip Electrical Power Subsystem Sizing

Parameter	Description	Assumed Value [22, 37]	Result	Equation
e	eccentricity	0 (circular)		
h	altitude	686 km		
$R_\oplus$	Earth radius	6378 km		
a	semi-major axis	7064 km		$a=h+R_\oplus$
P	period		98.5 min	(1)
$\mu_\oplus$	gravitational parameter	$3.986\text{x}10^5$ km^3/s^2		
ρ	Earth angular radius		64.5 deg	(2)
T_e	time in eclipse		35.7 min	(3)
T_s	time in sun		58.9 min	$T_s=P-T_e$
P_e	power required in eclipse	100 µW		
w	energy storage		214 mWs or mJ	$w=P_eT_e$
v	voltage	2.5V		
C	capacitance		68.5 mF	(4)
X_d	daytime conversion efficiency	0.85		
P_e	power required in eclipse	0		
P_{sa}	power required from array		1.33 mW	(5)
θ	average incidence angle	45°		
G_s	solar flux (average)	1358 W/m^2		
η	solar cell efficiency	1%		
I_d	inherent efficiency	100%		
P_{BOL}	beginning-of-life power		9.6 W/m^2	(6)
A_{sa}	**required solar array area**		**12x12 mm**	$A_{sa}=P_{sa}/P_{BOL}$

SpaceChip Data Handling Subsystem

Asynchronous system architecture, including a microcontroller core, is ideal for SpaceChip. Design hardening could be used for protection against the space radiation environment. In previous research, the author has investigated an asynchronous architecture specifically for space applications [39]. This combined approach offers a low-power radiation tolerant solution and eliminates the need for an external oscillator, but with a penalty in circuit complexity and area [40].

SpaceChip Communications Subsystem

The biggest challenge for satellite-on-a-chip is the communications link between the ground and the satellite. The onboard RF transmit power must be significant enough for an effective downlink. Early calculations revealed that the corresponding electrical power to generate the minimum downlink RF power would require an integrated solar array area of at least 50 cm^2, assuming 1% efficient cells. This is well outside of the 360 mm^2 maximum reticle area. Another challenge is that the ground station must know exactly where the satellite is to avoid pointing losses with its high gain antennas. Due to the very small size of SpaceChip, it is assumed that current space surveillance networks would have difficulty detecting and tracking it.

A strategy to meet these challenges is to avoid them altogether. A potential architecture would rely on a supporting co-orbital satellite that would serve as a relay to the ground station. SpaceChips with integrated transceivers could be distributed in nearby orbits with a maximum separation of a kilometer, similar to wide-area wireless sensor networks. Without propulsion, the mission lifetime would be determined by how long the SpaceChips could stay within communication range before drifting apart.

Table 3 summarizes the communication subsystem sizing process, using Eq. 7–8 to solve for the maximum data rate given a desired 1 km range. The result of 300 bps is very low, which assumes an external antenna is used. As discussed previously, an on-chip antenna would only have a range of 5 m [31]-[32].

$$L_s = \left(\frac{\lambda}{4\pi S}\right)^2 \tag{7}$$

$$\frac{E_b}{N_0} = \frac{P_t L_l G_t L_s L_a L_r L_p G_r}{k T_S R} \tag{8}$$

Environmental Operability and Survivability

The freefall environment of orbit introduces the potential need for attitude control, depending on the sensor and/or EPS requirements. If the sensor requires, at least two methods of semi-active control are possible. First, an on-chip electromagnet and sensor could be used, as demonstrated in [41]. A second option would use an on-chip magnetorquer coupled with passive aerodynamics via a "drag tail," which has been proposed for very small satellites [42]. Even if the sensor does not have pointing requirements, the EPS requires sunlight to generate power. Considering that the active circuit area is only on one side of the die, a solution to overcome this would be to sandwich two die together to guarantee illumination at any attitude.

Orbit and time determination may also be required when recording sensor measurements. Global Positioning System (GPS) receivers are a reliable method for determining spacecraft position and time for satellites. Single-chip solutions have been demonstrated, but even the best effort to date requires 56 mW, a few external passive elements, a precision crystal oscillator, and an antenna [43].

Table 3. SpaceChip Communication Subsystem Sizing

Parameter	Description	Assumed Value [38]	Result	Equation
P_t	transmitter power	1 μW		
L_l	line losses	0 dB		
G_t	transmitter gain	0 dB		
f	frequency	2.4 GHz		
c	speed of light	$3x10^8$ m/s		
λ	wavelength		0.125 m	$\lambda=c/f$
S	range	1 km		
L_s	free-space loss	-100 dB		(7)
L_a	atmospheric loss	0 dB		
L_r	rain loss	0 dB		
L_p	polarization loss	0 dB		
G_r	receiver gain	0 dB		
k	Boltzmann's constant	$1.381x10^{-23}$ J/K		
T_s	system noise	21.3 dB-K		
	modulation scheme	BPSK		
Minimum E_b/N_o	minimum for BPSK	9.6 dB		
Desired E_b/N_o	+10 dB margin	> 19.6 dB		
R	**data rate**		**300 bps**	(8)

Orbit control is not possible without propulsion. The most promising technology that may eventually be applicable for a SoC is the digital micro-propulsion effort [44]. At present, this technology requires a high activation voltage, cannot deliver symmetric thrust, and cannot be integrated monolithically in CMOS.

Finally, the unique thermal environment of space must be considered. The temperature extremes SpaceChip will experience were estimated as shown in Table 4 [34]. The TCS sizing process starts from the previous result of Eq. 2, then proceeds to model SpaceChip as a flat plat facing a round Earth using Eq. 9–12. The resulting temperature range of 96 to -74°C is concerning, indicating a large swing in temperatures during an orbit. However, this is not surprising for a very low mass system and is close to the range of industrial grade electronics (-40 to +85 °C). Sandwiching two die on a thermal substrate should simultaneously solve EPS attitude and TCS requirements.

$$F_P = \sin^2 \rho \tag{9}$$

$$K_a = 0.664 + 0.521\rho - 0.203\rho^2 \tag{10}$$

$$T_{\max} = \left[\frac{\alpha_t G_S + \varepsilon_b q_I F_P + \alpha_b a G_S K_a F_P - G_S \eta}{\sigma(\varepsilon_b + \varepsilon_t)} \right]^{1/4} \tag{11}$$

$$T_{\min} = \left[\frac{\varepsilon_b q_I F_P}{\sigma(\varepsilon_b + \varepsilon_t)} \right]^{1/4} \tag{12}$$

Table 5 summarizes the SpaceChip system requirements and verifies how they are met, based on the outcomes discussed throughout this section. A minimum configuration requires two die sandwiched together on a thermal substrate, an external antenna, and possibly a thin-film battery. Section 5 now discusses areas for further research and development to realize SpaceChip in CMOS.

Table 4. SpaceChip Thermal Subsystem Sizing

Parameter	Description	Assumed Value [35, 38]	Result	Equation
α	Si absorptivity	0.48		
ε	Si emissivity	0.46		
ρ	Earth angular radius		64.5 deg	(2)
F_p	flat plate view factor		0.86	(9)
K_a	spherical view factor		0.99	(10)
G_s	solar flux (max)	1418 W/m^2		
a	albedo	35%		
hot q_I	hot Earth IR	258 W/m^2		
σ	Stefan-Boltzmann constant	5.67x10^{-8} W/m^{2}K^4		
$\boldsymbol{T_{max}}$	**max temperature**		**96 °C**	(11)
cold q_I	cold Earth IR	216 W/m^2		
$\boldsymbol{T_{min}}$	**min temperature**		**-74 °C**	(12)

Table 5. SpaceChip System Requirements and Verification

System	Requirement	Outcomes
Top Level	-SpaceChip shall be implemented on a commercial CMOS process, suitable for integration of digital, analog, and RF components	-AMS 0.35 µm SiGe-BiCMOS
	-SpaceChip shall meet all mission objectives and support the ops concept	
Payload	-The payload shall be a CMOS imager	-Very limited payload options
	-Potential payload to detect plasma depletions shall be investigated	
Orbit	-SpaceChip shall be designed to operate in LEO orbits	-686 km/98 deg
Configuration & Structure	-Configuration shall be a monolithic "satellite-on-a-chip"	-18x20x3 mm
	-Size shall not exceed the typical 18x20 mm CMOS process reticle limit	-10 g
	-Mass shall be less than 10 g	-Two die sandwiched
	-The design shall incorporate a launch vehicle interface	
EPS	-Power source shall be solar energy via integrated photovoltaic cells	-1 mW budget
	-Secondary power source shall be investigated	-None possible
DH	-CPU shall be based on reduced instruction set microcontroller	-Hardened asynchronous microcontroller
	-Non-volatile memory technologies shall be investigated and addressed	
	-Radiation hardening shall be achieved by design hardening	
Comm	-2.4 GHz Instrumentation, Scientific, Measurement band shall be used	-1 µW, 1 km range
	-Each SpaceChip shall have a unique identification number	-Ext. antenna req'd
AOCS	-Attitude determination not required, passive shall be investigated	-Semi-active ADCS
	-Investigate orbit determination sensors	-GPS not possible
Propulsion	-Not required, technologies shall be investigated and assessed	-None possible
TCS	-Passive control shall be used	-Thermal substrate

5. RESEARCH AND DEVELOPMENT ROADMAP

The ultimate SoC vision for any application is a stand-alone product that can be used directly off the CMOS process line without any additional components, packaging, or interfaces. A survivable SoC has additional features and functional requirements as outlined in Section 3. Based on our experience with very small satellite design we have identified the following research areas that are worth pursuing further in order to realize a true SoC implementation of a survivable wireless sensor node:

(1) Sensors

(2) Power generation and storage

(3) Asynchronous system architecture

(4) Transceivers and antennas

(5) Attitude control

(6) Location and time determination

(7) Propulsion

(8) Environmental extremes tolerance

The Next Step: Pursuing SpaceChip

The discussion in Section 4 concluded that the requisite technologies are in place to support the design and demonstration of the first SpaceChip prototype. The target process for this work is the austriamicrosystems 0.35µ SiGe BiCMOS line through the EUROPRACTICE multi-project run service. We are currently using Cadence with the austriamicrosystems design kit and are also investigating newly available asynchronous synthesis tools.

Our aim is to not only help achieve the vision of a stand-alone SoC, but to design a system that can withstand hostile environments, particularly those encountered in space missions. Our focus is currently on developing and demonstrating four key capabilities:

Radiation Tolerant Asynchronous Microcontroller—Asynchronous microcontrollers and microprocessors, still considered a novelty, are just now commercially available as hardware or intellectual property cores. A more streamlined, flexible, and radiation tolerant design is required for SpaceChip.

Asynchronous design for space applications has only been considered by the author [39] and a handful of others. The challenge is that the asynchronous power efficiency gain is partially offset by power and area hungry design hardening techniques. The focus here will be to optimize this trade space. In addition, integrated flash memory will be considered to enhance the application flexibility as much as possible, as one of the SoC drawbacks is its inflexibility once realized in hardware. Being able to change the software should allow the same hardware to be used for a range of similar applications.

Power Generation via Solar Cells—Numerous integrated power sources have been studied, but all have remained elusive for commercial CMOS. Integrated solar cells seem to be the most relevant to SpaceChip. Of the few published attempts, only one has achieved an efficiency of one percent, which is well below the ideal [22]. In private communications with the authors of that work, they believe that improvements can be made, although they have shifted their focus elsewhere. A closer look at the device physics level is required to determine if this is a fruitful direction.

Stand-alone Transceiver—All SoC transceivers to date require external passive devices, precision frequency oscillators, and antennas. Research is needed to determine if a very simple transceiver, perhaps using OOK modulation, could be implemented on CMOS without any external components. However, it has been clearly demonstrated that an external antenna will be required when the ISM frequency bands are desired.

Spacecraft Configuration—A simple configuration, such as two die sandwiched together, could help meet EPS and TCS requirements. An investigation is required to determine the material composition and minimal packaging.

6. SUMMARY

Emerging wireless sensor network applications for hostile environments has prompted an investigation into survivable sensor node design techniques, which currently do not exist. These nodes must survive a range of mechanical, thermal, atmospheric, energetic, and dynamic extremes. Focusing on a system-on-a-chip design architecture, solutions were presented and discussed for each of these hazards.

An example SpaceChip scenario was presented, where the conceptual design of a satellite-on-a-chip was used to illustrate how a stand-alone system-on-a-chip could meet a range of unrealized distributed space mission requirements. The final SpaceChip configuration is composed of two solar-powered CMOS die sandwiched on a thermal control substrate. The only additional components required are an antenna and potentially a thin-film battery, depending on the mission requirements. The SpaceChip unit cost would be well below $500.

Further research is required to achieve the ultimate goal of complete system-on-a-chip solutions. For SpaceChip in particular, more research in radiation tolerant asynchronous microcontrollers, solar cells, stand-alone transceivers, and spacecraft configuration is needed. These research areas are our current focus at the Surrey Space Centre.

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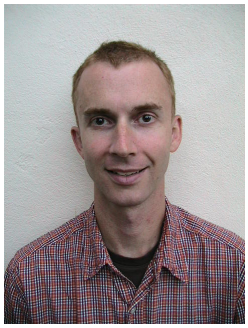
David Barnhart, MSEE, PE is a PhD candidate at the University of Surrey Space Centre in the United Kingdom. He was awarded an MS in Electrical Engineering, with a focus on VLSI design for space applications, by the Air Force Institute of Technology in 1999. He holds the rank of Major in the U.S. Air Force and most recently served as an Assistant Professor of Astronautics at the USAF Academy in Colorado, where he co-developed the EyasSAT Educational Satellite System and was the program manager of the student-built FalconSAT-2 microsatellite. His current research topic is "Very Small Satellite Design for Distributed Space Missions." After completing his Air Force sponsored university studies, he will return to space systems research and development before returning to USAF Academy. He is a member of the IEEE and Senior Member of the AIAA.



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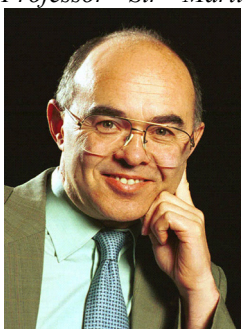
Professor Sir Martin N. Sweeting, B.Sc.Hons., PhD (Surrey), FRS, FREng., FIEE, FRAeS, FBIS, SMIEEE, SMAIAA, MBIM, MIAA has pioneered the concept of advanced microsatellites utilizing modern commercial-off-the-shelf (COTS) devices for 'affordable access to space.' After completing BSc & PhD degrees at the University of Surrey, in 1985 he formed a spin-off University company (SSTL - Surrey Satellite Technology Ltd) which has designed, built, launched and operates in orbit a total of 26 nano, micro, and mini-satellites - making SSTL the world's leading microsatellite company. As Chief Executive of SSTL, he has been responsible for the leadership and management of the Company which by 2006 has grown to 210 commercial staff and achieved a total export sales of over £110M. Sir Martin is also Director of the Surrey Space Centre, leading a team of 60 faculty and doctoral researchers investigating advanced small satellite concepts and techniques. Sir Martin was knighted by HM The Queen in the 2002 British New Year Honours for services to the small satellite industry.



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